**QPS-2110WG** **(RoHS Compliant)**

# 41.25Gbps / CWDM 4-λ QSFP+ LC SINGLE-Mode Optical Transceiver for 40GBASE-LR4

## FEATURES

- Up to 10.3125 Gbps Bi-directional Data Links Per Lane
- Compliant with SFF-8436 QSFP+ MSA
- Complaint with IEEE 802.3ba 40GBASE-LR4
- Hot Pluggable Electrical Interface
- Link Length up to 10km with SMF
- Uncooled CWDM 4-Wavelength DFB LDs: 1271, 1291, 1311, and 1331 nm
- 2-Wire Interface for Integrated Digital Diagnostic Monitoring
- Power Consumption < 3.5W
- Single +3.3V Power Supply
- RoHS 6/6 Compliant
- -5 to 70°C Case Operating Temperature
- Duplex LC Connector

## APPLICATIONS

- 40GBASE-LR4 (41.25Gbps)

## DESCRIPTION

QPS-2110WG series single mode QSFP+ transceiver is designed for single-mode fiber optical data communications such as 40GBASE-LR4.

The transceiver consists of two sections: The transmitter section consists of four directly modulated uncooled CWDM 4-λ 1271, 1291, 1311, and 1331 nm DFB lasers and four drivers. The receiver section incorporates four PIN photodiodes integrated with four trans-impedance preamplifiers (TIA) and four limiting post-amplifier ICs.

The module is with the QSFP+ 38-pin connector to allow hot plug capability. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. Only single 3.3V power supply is needed.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire QSFP+ Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

## LASER SAFETY

This single mode transceiver is a Class 1 laser product. It complies with IEC-60825-1 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

## ORDER INFORMATION

| P/No. | Bit Rate (Gb/s) | 40GBASE | Wavelength (nm) | Package | Connector | Temp (°C) | RoHS Compliant |
|---|---|---|---|---|---|---|---|
| QPS-2110WG | 41.25 | LR4 | CWDM 4-λ* | QSFP+ with DMI | LC | -5 to 70 | Yes |

CWDM 4-λ*: 1271, 1291, 1311, and 1331 nm DFB LDs.

**Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | Tstg | -40 | 85 | °C | |
| Operating Case Temperature | Topr | -5 | 70 | °C | |
| Relative Humidity | RH | 5 | 85 | % | Non condensing |
| Power Supply Voltage | $V_{CC}$ | -0.5 | 3.6 | V | |
| Data Input Voltage- Single Ended | --- | -0.5 | Vcc+0.5 | V | |

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| Recommended Operating Conditions | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Units / Notes** |
| Power Supply Voltage | $V_{CC}$ | 3.135 | 3.3 | 3.465 | V |
| Power Supply Current | $I_{CC}$ | | | 1000 | mA |
| Power Dissipation | $P_D$ | | | 3.5 | W |
| Operating Case Temperature | Topr | -5 | | 70 | °C |
| Data Rate | | | 41.25 | | Gb/s |

| Transmitter Optical Specifications (Topr= -5 to 70°C, Vcc3 = 3.3V ±5%) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Units** | **Notes** |
| Average Launch Power, each lane | $Po_{, Avg}$ | -7 | | 2.3 | dBm | 1 |
| Launch Power in OMA, each lane | $Po_{, OMA}$ | -4 | | 3.5 | dBm | |
| Total average launch power | $Po_{, Total}$ | | | 8.3 | dBm | |
| Difference in launch power between any two lanes in OMA | | | | 6.5 | dB | |
| Center Wavelength – lane 0 | $\lambda_{C0}$ | 1264.5 | 1271 | 1277.5 | nm | |
| Center Wavelength – lane 1 | $\lambda_{C1}$ | 1284.5 | 1291 | 1297.5 | nm | |
| Center Wavelength – lane 2 | $\lambda_{C2}$ | 1304.5 | 1311 | 1317.5 | nm | |
| Center Wavelength – lane 3 | $\lambda_{C3}$ | 1324.5 | 1331 | 1337.5 | nm | |
| Side Mode Suppression Ratio | SMSR | 30 | | | dB | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| Transmitter and Dispersion Penalty, each lane | TDP | | | 2.6 | dB | 2 |
| Optical Eye Mask | Compliant with IEEE 802.3ba 40GBASE | | | | | |
| Average Launch Power of OFF Transmitter | | | | -30 | dBm | |

1. Output power is power coupled into a 9/125 μm single-mode fiber.
2. Measured with a PRBS $2^{31}$-1 test pattern @10.3125 Gbps.

| Receiver Optical Specifications (Topr= -5 to 70°C, Vcc3 = 3.3V ±5%) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Units** | **Notes** |
| Average receive power, each lane | Sen1 | -13.7 | --- | 2.3 | dBm | 3 |
| Receiver power (OMA), each lane | Sen2 | -11.5 | --- | 3.5 | dBm | |
| Stress receiver sensitivity (OMA), each lane | Sen3 | | | -9.6 | | |
| Difference in receive power between any two lanes (OMA) | | | | 7.5 | dB | |
| Damage Threshold | | 3.3 | --- | | dBm | |
| LOS -- Deasserted | $LOS_D$ | --- | --- | -14 | dBm | Transition: low to high |
| LOS -- Asserted | $LOS_A$ | -28 | --- | --- | dBm | Transition: high to low |
| LOS -- Hysteresis | | 0.5 | --- | | dB | |
| Wavelength of Operation – lane 0 | $\lambda_{C0}$ | 1264.5 | | 1277.5 | nm | |
| Wavelength of Operation – lane 1 | $\lambda_{C1}$ | 1284.5 | | 1297.5 | nm | |
| Wavelength of Operation – lane 2 | $\lambda_{C2}$ | 1304.5 | | 1317.5 | nm | |
| Wavelength of Operation – lane 3 | $\lambda_{C3}$ | 1324.5 | | 1337.5 | nm | |
| Receiver reflectance (max) | | | | -26 | dB | |

3. Average received power @ BER=1E-12 and PRBS $2^{31}$-1.

| Electrical Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Units** | **Notes** |
| **High-Speed Signal (CML) Interface Specification** | | | | | | |
| Input Data Rate | | | 10.3125 | | Gps | |
| Differential Input Impedance | Rin | | 100 | | Ω | |
| Differential Data Input Amplitude | | 200 | | 800 | mVpp | Internally AC coupled |
| Output Data Rate | | | 10.3125 | | Gps | |
| Differential Output Impedance | Rout | | 100 | | Ω | |
| Differential Data Output Amplitude | | 300 | | 900 | mVpp | Internally AC coupled |
| **Low-Speed Signal (LVCMOS) Interface Specification** | | | | | | |
| Input High Voltage | | Vcc*0.7 | | Vcc+0.5 | V | |
| Input Low Voltage | | -0.3 | | Vcc*0.3 | V | |
| Output High Voltage | | Vcc-0.5 | | Vcc+0.3 | V | |
| Output Low Voltage | | 0 | | 0.4 | V | |
| **Low-Speed Signal (LVTTL) Interface Specification** | | | | | | |
| Input High Voltage | | 2.0 | | Vcc+0.3 | V | |
| Input Low Voltage | | -0.3 | | 0.8 | V | |
| Output High Voltage | | Vcc-0.5 | | Vcc+0.3 | V | |
| Output Low Voltage | | 0 | | 0.4 | V | |

## MANAGEMENT INTERFACE

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128*256 = 32 Kbytes in this upper memory space. Please refer SFF-8436 (Revision 4.1) for detailed information.

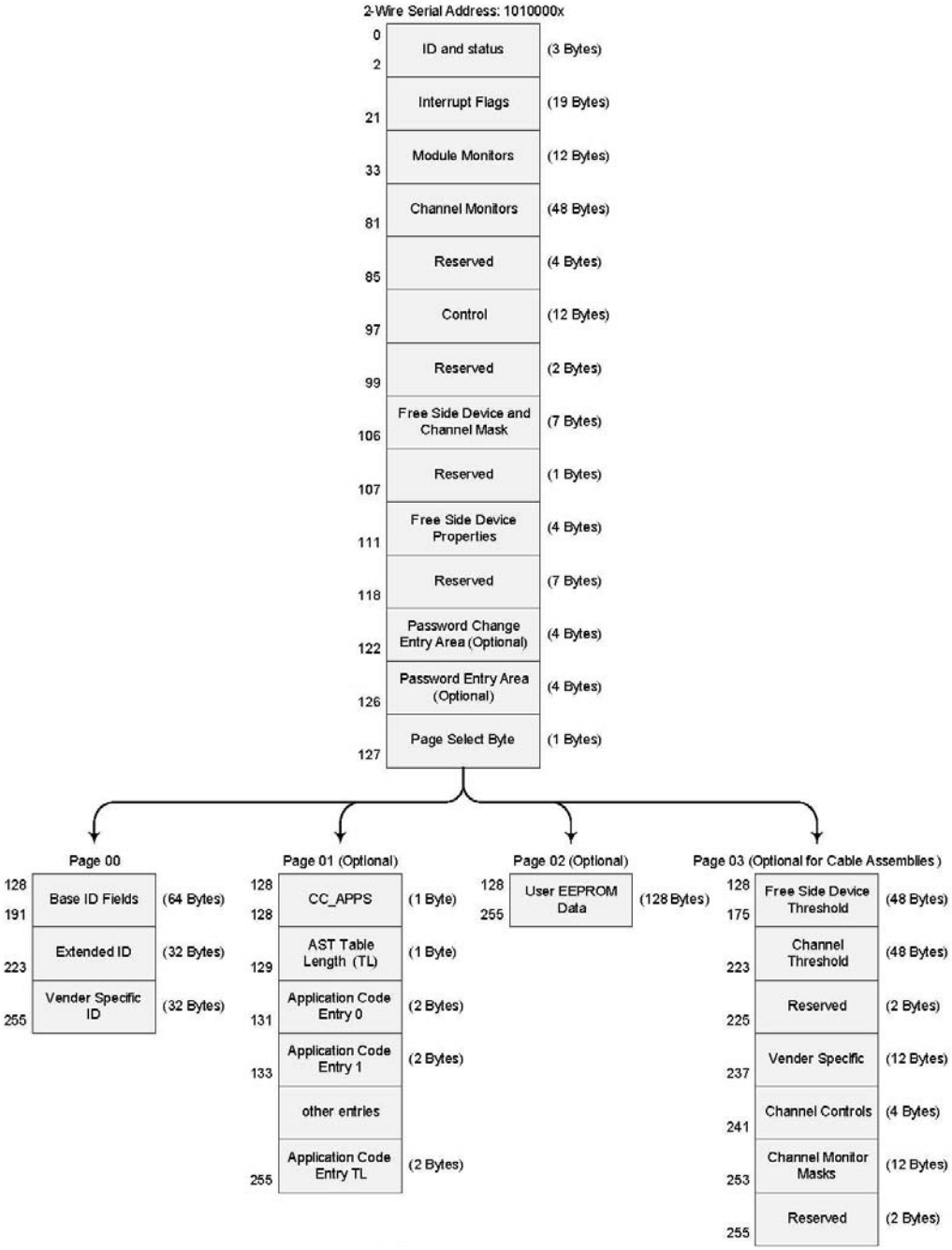



Figure 1. 2-wire Serial Digital Diagnostic Memory Map

CONNECTION DIAGRAM

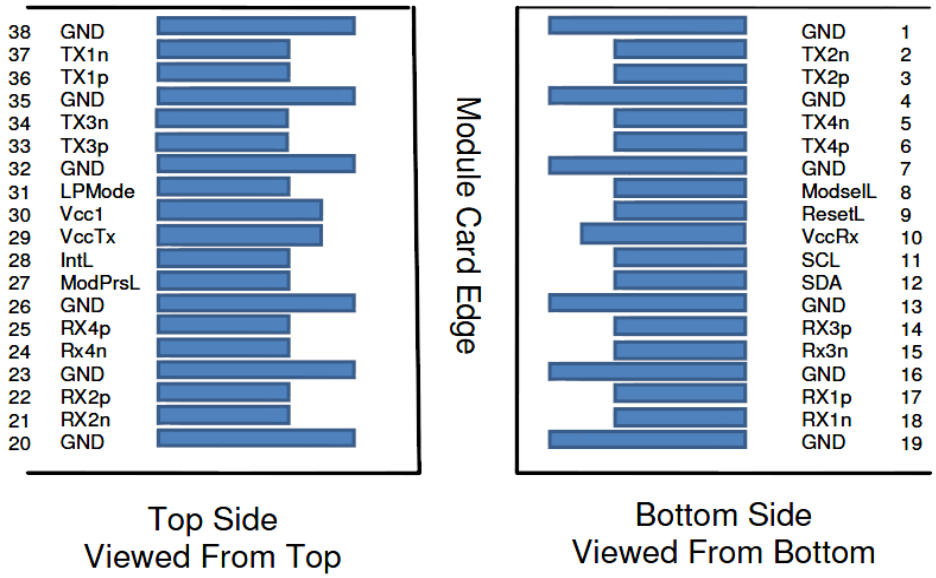


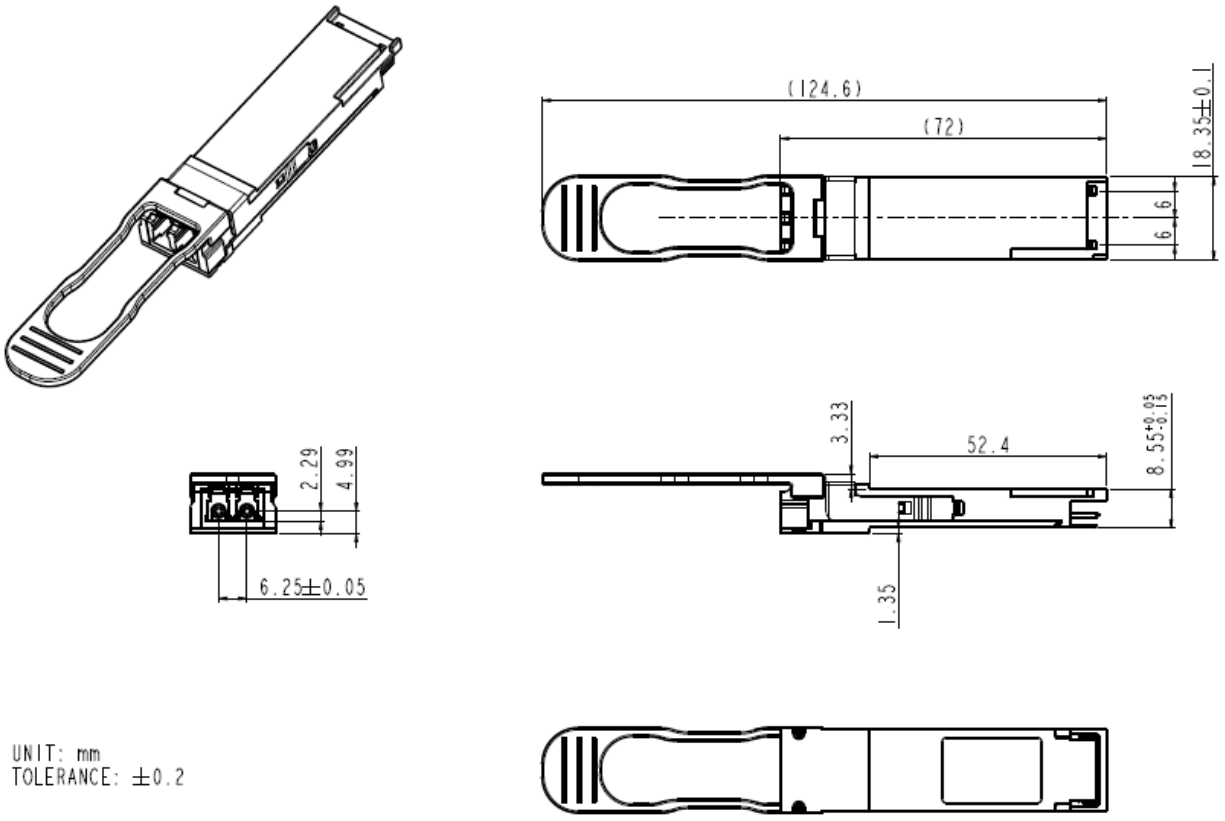

**Table 3 PIN Description**

| PIN | Logic | Signal Name | Description | Note |
|---|---|---|---|---|
| 1 | | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | |
| 4 | | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | |
| 7 | | GND | Ground | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | |
| 9 | LVTTL-I | ResetL | Module Reset | |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver | 2 |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | |
| 13 | | GND | Ground | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | | GND | Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | |
| 28 | LVTTL-O | IntL | Interrupt | |
| 29 | | Vcc Tx | +3.3V Power supply transmitter | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2 |
| 31 | LVTTL-I | LPMode | Low Power Mode | |
| 32 | | GND | Ground | 1 |

| | | | | |
|---|---|---|---|---|
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | |
| 35 | | GND | Ground | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | |
| 38 | | GND | Ground | 1 |

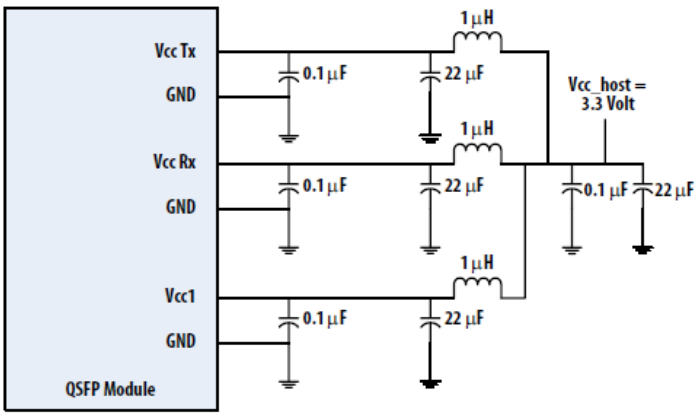
1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination.

## MECHANICAL SPECIFICATION (UNITS IN MM)




**Note:** Specifications subject to change without notice.

RECOMMENDED POWER CIRCUIT SCHEMATIC




RECOMMENDED INTERFACE CIRCUIT

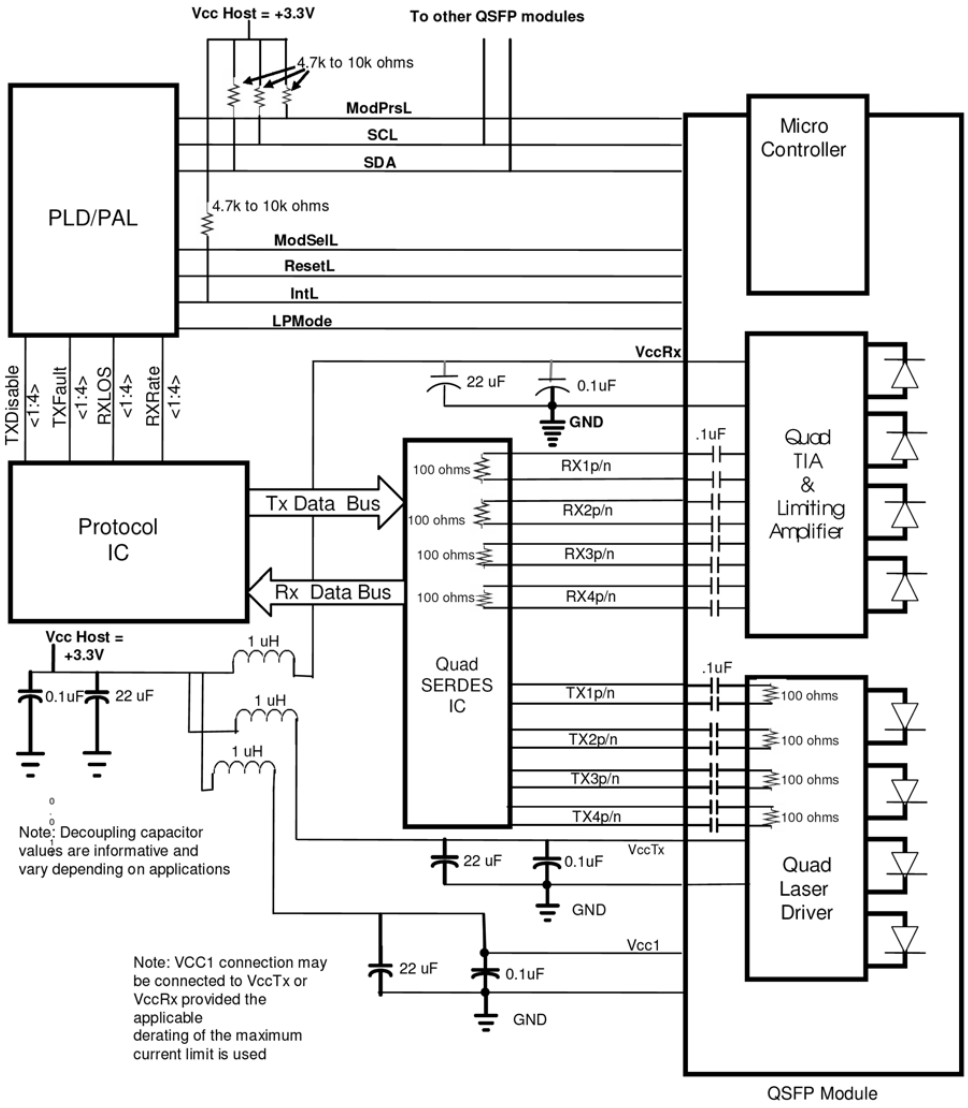


**Table 4 Serial ID Memory Contents (Page 00h)**

| Address | Field Size (Byte) | Name of Filed | Description | Hex |
|---|---|---|---|---|
| 128 | 1 | Identifier | QSFP+ | 0D |
| 129 | 1 | Ext. Identifier | power consumption <3.5W, no CLEI code, no CDR in TX, no CDR in RX | C0 |
| 130 | 1 | Connector type | LC | 07 |
| 131~138 | 8 | Transceiver | 40GBASE-LR4, 1000BASE-LX, Fibre Channel Long Distance (L), Longwave Laser (LL), Single Mode (SM), 1200 Mbytes/sec | 02 00 00 02 10 10 01 80 |
| 139 | 1 | Encoding | 64B66B, | 05 |
| 140 | 1 | BR, nominal | 10.3Gbps | 67 |
| 141 | 1 | Extended Rate Select | Not supported | 00 |
| 142 | 1 | length (SMF)-km | 10 km | 0A |
| 143 | 1 | Length (OM3) | 0 m | 00 |
| 144 | 1 | Length (OM2) | 0 m | 00 |
| 145 | 1 | Length (OM1) | 0 m | 00 |
| 146 | 1 | Length (Copper) | 0 m | 00 |
| 147 | 1 | Device Tech | 4-Wavelength CWDM 1270 nm to 1330 nm DFB LD, No Wavelength Ctrl, Uncooled TX, PIN detector, TX not tunable | 40 |
| 148~163 | 16 | Vendor name | OPTOWAY | 4F 50 54 4F 57 41 59 20 20 20 20 20 20 20 20 20 |
| 164 | 1 | InfiniBand Compliance | | 00 |
| 165~167 | 3 | Vendor OUI | | 00 0E FA |
| 168~183 | 16 | Vendor PN | QPS-2110WG | 51 50 53 2D 32 31 31 30 57 47 20 20 20 20 20 20 |
| 184~185 | 2 | Vendor rev | ASCII (“31 61” means 1a revision) | xx xx |
| 186~187 | 2 | Wavelength | 1301 nm (4-Wavelength CWDM 1270 nm to 1330 nm DFB LD) | 65 A4 |
| 188~189 | 2 | Wavelength Tolerance | +/- 36.5nm | 1C 84 |
| 190 | 1 | Max Case Temp | 70deg | 46 |
| 191 | 1 | CC_BASE | Check sum of Byte 128 -- 190 | |
| 192~195 | 4 | Options | Page 02/01 not supported | 00 00 00 D8 |
| 196~211 | 16 | Vendor SN | ASCII | xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx |
| 212~219 | 8 | Date code | ASCII Year (2 Byte), Month (2 Byte), Day (2 Byte) | xx xx xx xx xx xx 20 20 |
| 220 | 1 | Diagnostic Monitoring Type | RX: Average Power | 08 |
| 221 | 1 | Enhanced Options | Not supported | 00 |
| 222 | 1 | Reserved | | 00 |
| 223 | 1 | CC_EXT | Check sum of Byte 192 -- 222 | |
| 224~255 | 32 | Vendor Specific | | 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 |

REVISION HISTORY

| Version | Subject | Release Date |
|---|---|---|
| 1.0 | Initial datasheet | 2016/1/25 |
| | | |
| | | |