

AFBR-57E6APZ

Multimode Small Form Factor Pluggable Transceivers with LC Connector and DMI for FDDI and Fast Ethernet



Data Sheet



Description

The AFBR-57E6APZ Small Form Factor Pluggable LC transceiver from Avago Technologies provides the system designer a product to implement FDDI/Fast Ethernet networks with DMI physical layers.

As an enhancement to the conventional SFP interface defined in SFF-8074i, the AFBR-57E6APZ is compatible to SFF-8472 (digital diagnostic interface for optical transceivers). Using the 2-wire serial interface defined in the SFF-8472 MSA, the AFBR-57E6APZ provides real time information on temperature, LED bias current, LED average output power and receiver average input power. The interface also adds the ability to monitor the Receiver Loss of Signal (RX_LOS).

Transmitter

The transmitter contains a 1310nm InGaAsP LED. This LED is packaged in the optical subassembly of the transmitter. It is driven by an integrated circuit which converts differential PECL logic signals into an analog LED drive current. This current is monitored by the digital diagnostic interface. The transmitter light output power is inferred from this information.

The LED is switched off in case a static signal is present at the PECL inputs.

Receiver

The receiver utilizes an InGaAs PIN photodiode coupled to a transimpedance pre- and postamplifier IC. It is packaged in the optical subassembly of the receiver. The data output is differential LVPECL. The LOS output is +3.3 V TTL as per SFF-8074i. The PIN photodiode average current is monitored by the digital diagnostic interface as a measure for input optical power. Rx squelch is activated when a low input power is detected.

Features

- RoHS compliant
- Lead free
- Industry standard Small Form Pluggable (SFP) package
- LC duplex connector optical interface
- Operates with 50/125 μ m and 62.5/125 μ m multimode fiber
- Compatible with 100Base-FX version of IEEE802.3u
- Single +3.3V power supply
- +3.3V TTL LOS output
- Squelched receiver outputs
- Manufactured in an ISO 9001 certified facility
- Operating temperature range: -40°C to 85°C
- Bail de-latch
- Hot plug capability

Applications

- Factory automation at Fast Ethernet speeds
- Fast Ethernet networking over multimode fiber.

Loss of Signal

The Loss of Signal (LOS) output indicates that the optical input power to the receiver does not meet the minimum detectable level for FDDI compliance.

Module package

The transceiver package is compliant with the Small Form Pluggable (SFP) MSA with the LC duplex connector option. The hot-pluggable capability of the SFP package allows the module to be installed at any time including when the host system is on-line and operating. This permits the system to be configured or maintained without system downtime. The AFBR-57E6APZ requires a 3.3V DC power supply for optimal performance.

Module Diagrams

Figure 1 illustrates the major functional components of the AFBR-57E6APZ. The connection diagram of the module is shown in Figure 2. Figures 5 to 7 depict the external configuration and dimensions of the module.

Installation

The AFBR-57E6APZ can be installed in or removed from any MultiSource Agreement (MSA) – compliant Small Form Pluggable port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical interface first, under finger pressure. Controlled hot-plugging is ensured by 3-stage pin sequencing at the electrical interface. The module housing makes initial contact with the host board EMI shield mitigating potential damage due to Electro-Static Discharge (ESD). The 3-stage pin contact sequencing involves (1) Ground, (2) Power, and then (3) Signal pins making contact with the host board surface mount connector in that order.

This printed circuit board card edge connector is depicted in Figure 2.

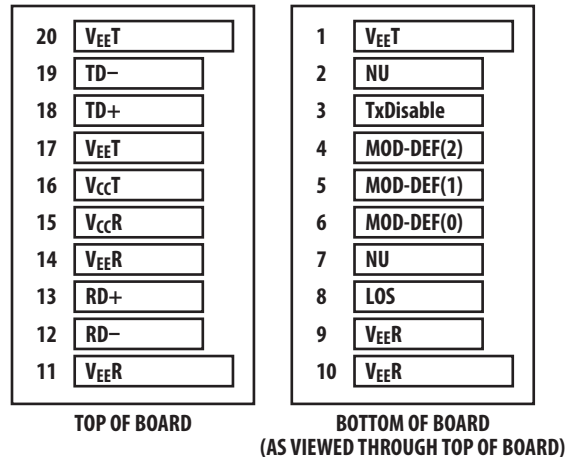


Figure 2. Connection diagram of module printed circuit board.

Digital Diagnostic Interface and Serial Identification

The 2-wire serial interface is based on ATMEL AT24C02C series EEPROM protocol. Conventional EEPROM memory (bytes 0-255 at memory address 0xA0) is organized in compliance with SFF-8074i. As an enhancement the AFBR-57E6APZ is also compatible to SFF-8472. This enhancement offers digital diagnostic information at bytes 0-255 at memory address 0xA2.

In addition to monitoring of the LED drive current and photodiode current, the interface also monitors the transmitter supply voltage and the temperature. The transmitter voltage supply must be provided for the digital diagnostic interface to operate.

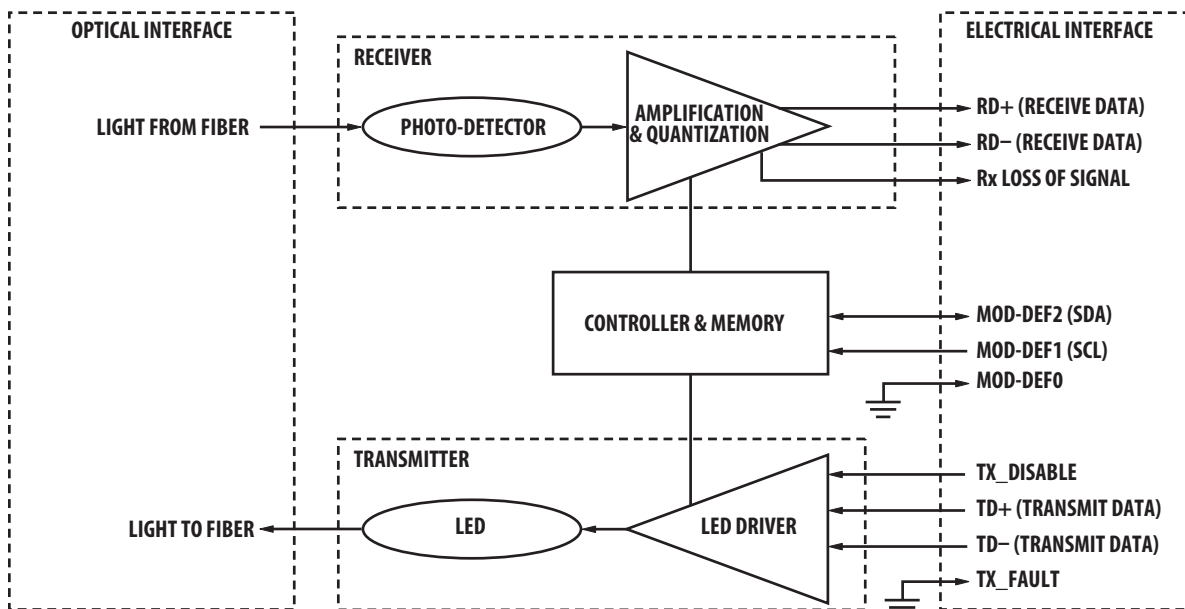


Figure 1. Transceiver functional diagram

Data I/O

The AFBR-57E6APZ fiber-optic transceiver is designed to accept industry standard differential signals. The transceiver provides an AC-coupled, internally terminated data interface. Coupling capacitors have been included within the module to reduce the number of components on the customer's board. Figure 3 depicts the recommended interface circuitry.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions where immunity to ESD damage is important. Table 1 documents the transceiver's immunity to both these conditions.

The first condition is static discharge to the transceiver when handling it. For example when the transceiver is inserted into the transceiver port. To protect the transceiver, it is important to use normal ESD handling procedures. These precautions include grounded wrist straps, workbenches, and floor mats in ESD controlled areas. The ESD sensitivity of the AFBR-57E6APZ is compatible with typical industry production environments.

The second condition is static discharge to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD events. The ESD performance of AFBR-57E6APZ exceeds typical industry standards.

Immunity

Equipment hosting the AFBR-57E6APZ will be subjected to radio-frequency electromagnetic fields in some environments. These transceivers have good immunity to such fields due to their shielded design.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of CENELEC EN55022.

The metal housing design and shielded design of the AFBR-57E6APZ transceiver minimize the EMI challenge facing the host equipment designer. The transceivers provide superior EMI performance.

Eye Safety

These transceivers provide Class 1 eye safety by design. Avago has tested the transceiver design for compliance with the requirements listed in Table 1 under normal operating conditions and under a single fault condition.

Flammability

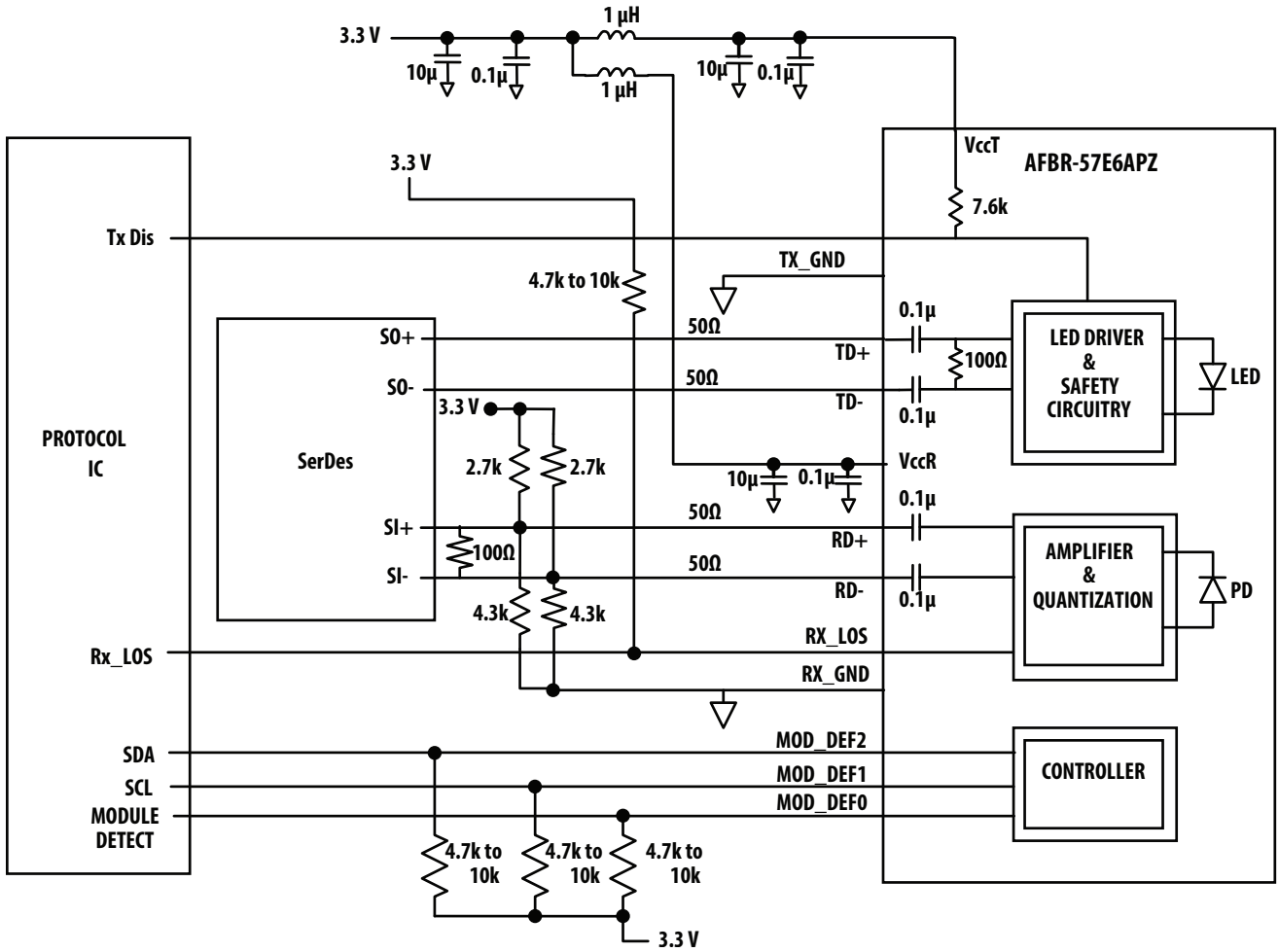
The AFBR-57E6APZ transceiver housing is made of metal and high strength, heat resistant, chemically resistant and UL-94V-0 flame retardant plastic.

Shipping Container

10 transceivers are packaged in one shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

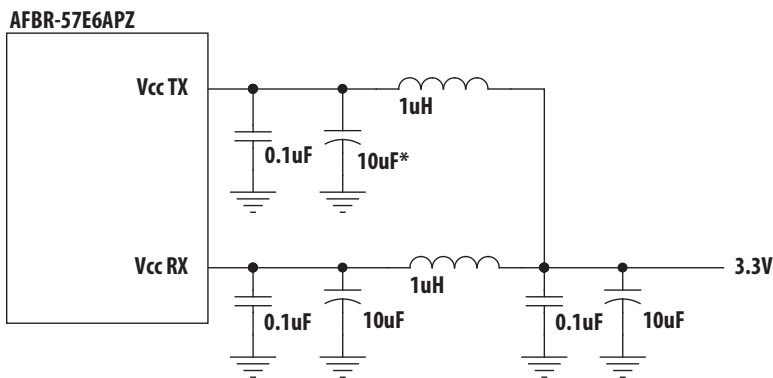
Table 1. Regulator Compliance

| Feature | Test Method | Performance |
|---|---|---|
| Electrostatic Discharge (ESD) to the electrical pins | Jedec JESD22-A114 | Meets Class 2 (2000 to 3999Volts). Withstand up to 2000V applied between electrical pins. |
| Electrostatic Discharge (ESD) to the Duplex LC Receptacle | Variation of IEC 61000-4-2 | Typically withstand at least 9kV without damage when the LC connector receptacle is contacted by a Human Body Model probe. Typically withstand 15kV air discharge on LC-connector receptacle. |
| Electromagnetic Interference (EMI) | FCC Class B, CENELEC EN55022 (CISPR 22) Class B | System margins are dependent on customer board and chassis design. |
| Immunity | IEC 61000-4-3 | Typically shows no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the transceiver without a chassis enclosure. |
| Component Recognition | Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment | E173874, Vol. 1 |
| Eye Safety | EN 60950-1:2006+A11+A1+A12+A2 EN 60825-1:2007 EN 60825-2:2004+A1+A2 | Compliant per Avago testing under single fault conditions. |
| RoHS Compliance | | Reference to RoHS Directive 2011/65EU Annex II |



Note:
 Please refer to SerDes supplier's recommendation regarding the interface between the AFBR-57E6APZ and the SerDes.
 The proposed termination is a general recommendation for LVPECL AC-coupled signals.
 Other terminations could also be applicable depending on the SerDes interface.

Figure 3. Recommended connection circuitry



Note: Inductors should have less than 1 Ohm series resistor per MSA
 * optional capacitance but recommended (required for SFP+)

Figure 4. MSA required power supply filter

Table 2. Pin Description

| Pin | Name | Function/Description | MSA Notes |
|-----|-------------------|---|-----------|
| 1 | V _{EE} T | Transmitter Ground | 1 |
| 2 | NU | Not Used | 2 |
| 3 | Tx Disable | Transmitter Disable – Module disables on high or open | |
| 4 | MOD-DEF2 | Module Definition 2 – Two wire serial ID interface | 3 |
| 5 | MOD-DEF1 | Module Definition 1 – Two wire serial ID interface | 3 |
| 6 | MOD-DEF0 | Module Definition 0 – grounded in module | 3 |
| 7 | NU | Not Used | |
| 8 | LOS | Loss of Signal – high indicates loss of signal | 4 |
| 9 | V _{EE} R | Receiver Ground | 1 |
| 10 | V _{EE} R | Receiver Ground | 1 |
| 11 | V _{EE} R | Receiver Ground | 1 |
| 12 | RD- | Inverse Received Data Out | 5 |
| 13 | RD+ | Received Data Out | 5 |
| 14 | V _{EE} R | Receiver Ground | 1 |
| 15 | V _{CC} R | Receiver Power 3.3V | |
| 16 | V _{CC} T | Transmitter Power 3.3V | |
| 17 | V _{EE} T | Transmitter Ground | 1 |
| 18 | TD+ | Transmitter Data In | 6 |
| 19 | TD- | Inverse Transmitter Data In | 6 |
| 20 | V _{EE} T | Transmitter Ground | 1 |

Notes:

1. Transmitter and Receiver grounds are connected in the transceiver PCB.
2. Pulled to <0.8V during transceiver operation.
3. Mod-Def 0, 1, 2 are the module definition pins. They should be pulled up with a 4.7kΩ to 10kΩ resistor on the host board to a supply less than V_{CC}T + 0.3V or V_{CC}R +0.3V. In order to use this interface, supply 3.3V to V_{CC}T.
Mod-Def 0 is grounded by the module to indicate that the module is present.
Mod-Def 1 is the clock line of the two-wire serial interface.
Mod-Def 2 is the data line of the two-wire serial interface.
4. LOS (Loss Of Signal) is an open collector/drain output which should be pulled up externally with a 4.7kΩ to 10 kΩ resistor on the host board to a supply less than V_{CC}T,R +0.3V. When high, this output indicates that the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). In the low state, the output will be pulled to a voltage less than 0.8V. LOS only valid if V_{CC}T and V_{CC}R are powered.
5. RD-/+: These are the differential receiver outputs. They are AC-coupled to 100Ω differential lines which should be terminated with 100Ω differential at the SERDES. AC-coupling is present inside the module and is not required on the host board.
6. TD-/+: These are the differential transmitter inputs. They are AC-coupled differential lines with 100Ω differential termination inside the module. AC-coupling is present inside the module and is not required on the host board.

Package Dimensions

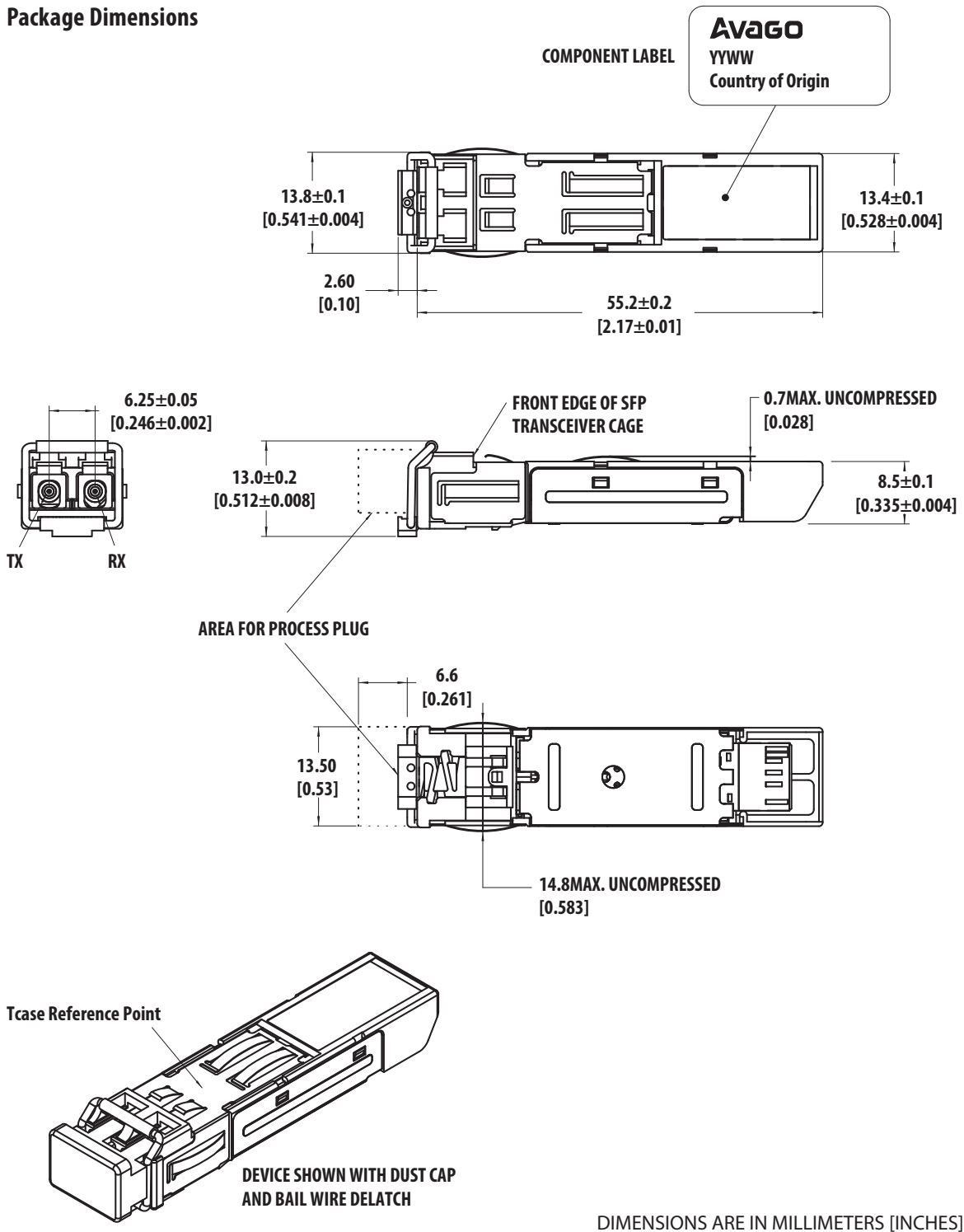
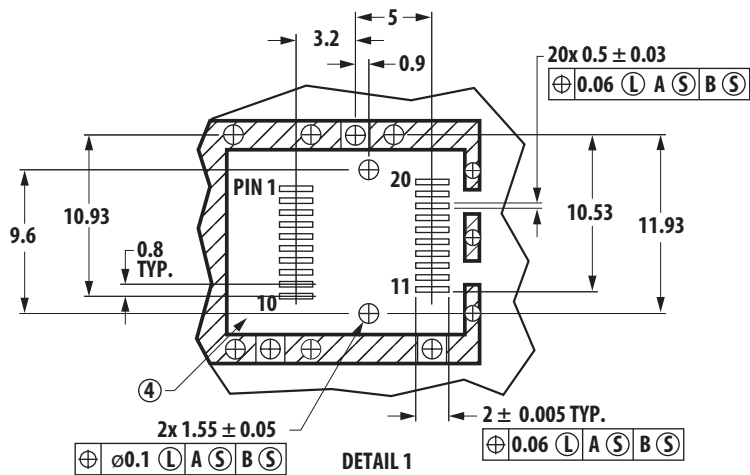
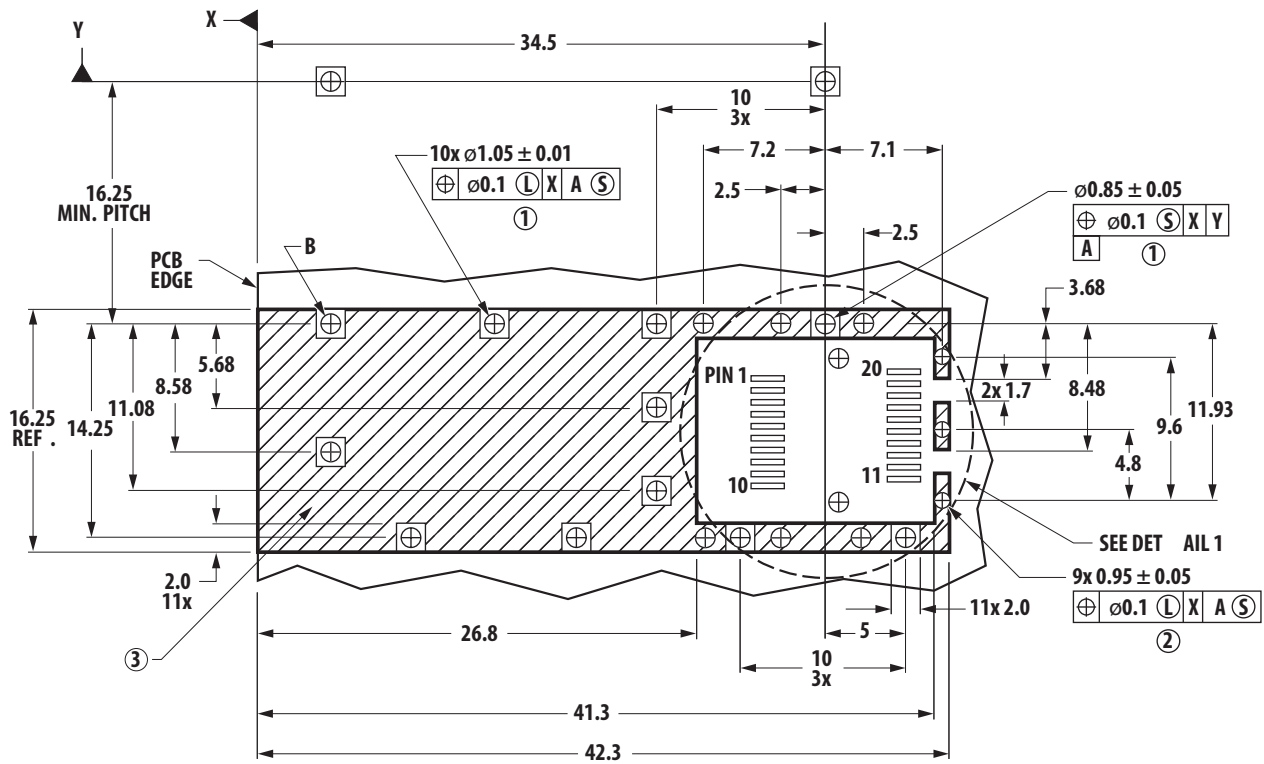


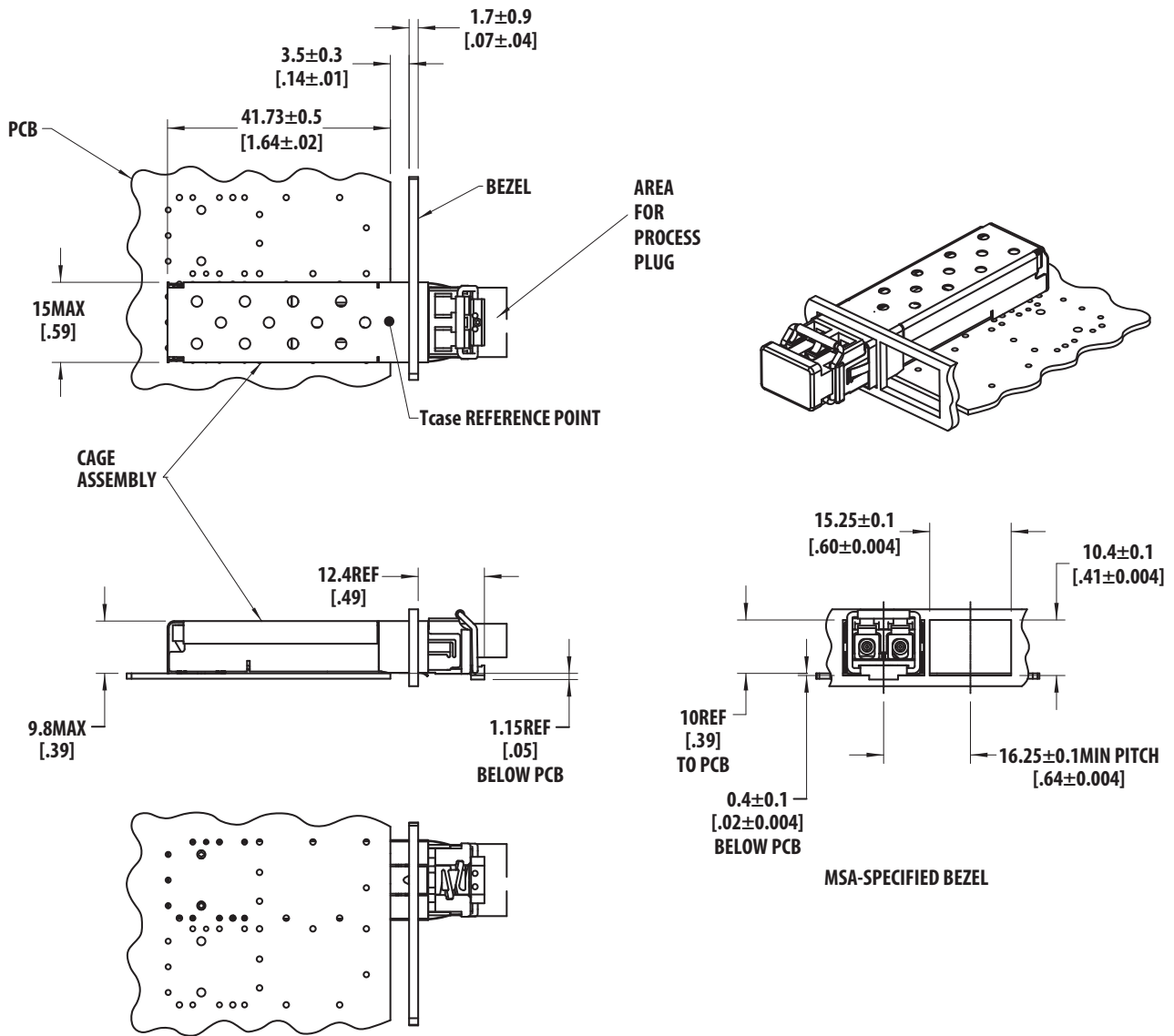
Figure 5. Module Drawing



LEGEND

1. PADS AND VIAS ARE CHASSIS GROUND
 2. THROUGH HOLES, PLATING OPTIONAL
 3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND)
 4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED)
- DIMENSIONS ARE IN MILLIMETERS

Figure 6. SFP Host Board Mechanical Layout



DIMENSIONS ARE IN MILLIMETERS [INCHES].

Figure 7. SFP Assembly Drawing

Table 3. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit | Notes |
|------------------------------|----------|------|----------|------|-------|
| Storage Temperature | T_S | -40 | +100 | °C | |
| Supply Voltage | V_{CC} | -0.5 | 3.63 | V | |
| Data Input Voltage | V_I | -0.5 | V_{CC} | V | |
| Receiver Optical Input Power | P_{in} | | 0 | dBm | |

Table 4. Recommended Operating Conditions

All the data in this specification refers to the operating conditions above and over lifetime unless otherwise stated.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---------------------------------|----------|-----|-----|-----|----------|--------------|
| Case Operating Temperature | T_C | -40 | | +85 | °C | 1, 2 |
| Supply Voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V | |
| Data Output Load | R_L | | 100 | | Ω | Differential |
| Signalling rate (Fast Ethernet) | B | | 125 | | MBd | 3 |

Table 5. Transmitter Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---------------------------------------|------------|-----|-----|----------|----------|-------|
| Supply Current | I_{CC} | | 45 | 70 | mA | 4 |
| Power Dissipation | P_{DISS} | | 150 | 260 | mW | |
| Differential input voltage | V_{DIFF} | 0.5 | 1.0 | 1.8 | V | 5 |
| Input Differential Impedance | R_{in} | | 100 | | Ω | 6 |
| Transmitter Disable (TX Disable) High | V_{IH} | 2.0 | | V_{CC} | V | |
| Transmitter Disable (TX Disable) Low | V_{IL} | 0 | | 0.8 | V | |

Table 6. Receiver Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|-------------------|-----|-----|-----|------|-------|
| Supply Current | I_{CC} | | 31 | 40 | mA | 4 |
| Power Dissipation | P_{DISS} | | 105 | 145 | mW | |
| Data Output: Receiver Differential Output Voltage (RD+/-) | $ V_{OH}-V_{OL} $ | 1.0 | | 1.8 | V | 7, 8 |
| Data Output Rise Time (10%-90%) | t_r | | | 2.2 | ns | |
| Data Output Fall Time (10%-90%) | t_f | | | 2.2 | ns | |
| Loss of Signal Output Voltage - Low | LOS_{VOL} | | | 0.8 | V | |
| Loss of Signal Output Voltage - High | LOS_{VOH} | 2.0 | | | V | |

Table 7. Transmitter Optical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---------------------|-------|-------|-------|------|--------|
| Output Optical Power 62.5/125µm NA = 0.275 Fiber | P _o | -20.0 | -17.0 | -14.0 | dBm | 9, 13 |
| Output Optical Power 50/125µm NA = 0.20 Fiber | P _o | -24.0 | -21.0 | -17.0 | dBm | 9, 13 |
| Extinction Ratio | ER | 10 | | | dB | |
| Central Wavelength | λ _C | 1270 | 1308 | 1380 | nm | |
| Spectral width – FWHM | Δλ | | 147 | | nm | |
| Optical Rise Time (10%-90%) | t _r | 0.6 | 1.0 | 3.0 | ns | 15 |
| Optical Fall Time (10%-90%) | t _f | 0.6 | 1.0 | 3.0 | ns | 15 |
| Duty Cycle Distortion Contributed by the Transmitter | DCD | | | 0.6 | ns | 10, 11 |
| Data Dependent Jitter Contributed by the Transmitter | DDJ | | | 0.6 | ns | 10 |
| Random Jitter Contributed by the Transmitter | RJ | | | 0.69 | ns | 5, 10 |
| Transmitter Disable (High) | P _{o(off)} | | | -45 | dBm | |

Table 8. Receiver Optical and Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|---------------------------------|-------|-----|-------|------|--------|
| Optical Input Power | P _{IN} | -31.0 | | -12.0 | dBm | 12, 13 |
| Operating Wavelength | λ _R | 1270 | | 1380 | nm | |
| Duty Cycle Distortion Contributed by the Receiver | DCD | | | 0.4 | ns | 14, 10 |
| Data Dependent Jitter Contributed by the Receiver | DDJ | | | 1.0 | ns | 10 |
| Random Jitter Contributed by the Receiver | RJ | | | 2.14 | ns | 5, 10 |
| Loss of Signal – De-asserted | P _D | | | -32.0 | dBm | 13 |
| Loss of Signal - Asserted | P _A | -45 | | | dBm | 13 |
| Loss of Signal – Hysteresis | P _A – P _D | 0.5 | 1.6 | | dB | |

Notes:

- The case temperature is measured at the surface of the topside (see figure5 Module drawing) using a thermocouple connected to the housing.
- Electrical and optical specifications of the product are guaranteed across recommended case operating temperature only.
- 4B/5B. Ethernet auto-negotiation pulses are not supported
- Typical Values are for room temperature at 3.3V.
- Peak to Peak.
- Tx data inputs are AC coupled.
- Differential output voltage is internally AC-coupled. The low and high voltages are measured using 100Ohm differential termination.
- RD+ and RD- outputs are squelched at LOS assert levels.
- Optical values are measured over the specified operating voltage and temperature ranges. The average power can be converted to a peak value by adding 3dB.
- Characterized with 125MBd, PRBS2⁷-1 pattern.
- Duty Cycle Distortion contributed by the transmitter is measured at 50% threshold of the optical signal.
- This specification is intended to indicate the performance of the receiver section of the transceiver when Optical Input Power signal characteristics are present per the following definitions:
 - Over the specified operating temperature and voltage ranges
 - Bit Error Rate (BER) is better than or equal to 1x10⁻¹⁰
 - Transmitter is operating to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
 - Fiber: 62.5/125 _m, NA = 0.275; or 50/125 _m, NA = 0.20
- Average
- Duty Cycle Distortion contributed by the receiver is measured at 50% threshold of the electrical signal.
- Measured with a 400MHz optical to electrical converter.

Table 9. Transceiver diagnostics timing characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|------------------------------------|----------------------------|-----|------|------|------------------|
| Hardware TXDIS Assert Time | t _{off} | | 10 | μs | Note 1, Figure 8 |
| Hardware TXDIS De-Assert Time | t _{on} | | 30 | μs | Note 2, Figure 8 |
| Time to Initialize | t _{init} | | 300 | ms | Note 3, Figure 8 |
| Hardware LOS Assert Time | t _{loss_on} | | 100 | μs | Note 4 |
| Hardware LOS De-Assert Time | t _{loss_off} | | 350 | μs | Note 5 |
| Software TX_DISABLE Assert Time | t _{off_soft} | | 100 | ms | Note 6 |
| Software TX_DISABLE De-Assert Time | t _{on_soft} | | 100 | ms | Note 7 |
| Software RX_LOS Assert Time | t _{loss_on_soft} | | 100 | ms | Note 8 |
| Software RX_LOS De-Assert Time | t _{loss_off_soft} | | 100 | ms | Note 9 |
| Analog parameter Data Ready | t _{data} | | 1000 | ms | Note 10 |
| Serial Hardware Ready | t _{serial} | | 300 | ms | Note 11 |
| Write Cycle Time | t _{write} | | 10 | ms | Note 12 |
| Serial ID Clock Rate | f _{serial_clock} | | 400 | kHz | Note 13 |

Notes:

1. Time from rising edge of TXDIS to when the optical output falls below 10% of nominal.
2. Time from falling edge of TXDIS to when the modulated optical output rises above 90% of nominal.
3. Time from Power on or falling edge of TXDIS to when the modulated optical output rises above 90% of nominal.
4. Time from loss of optical signal to LOS assertion.
5. Time from valid optical signal to LOS de-assertion.
6. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
7. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the modulated optical output rises above 90% of nominal.
8. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
9. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
10. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
11. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
12. Time from stop bit to completion of a 1-8 byte write command.
13. It is not recommended to continuously read the A2 EEPROM for more than 20 ms without a minimum time pause interval of 20 ms.

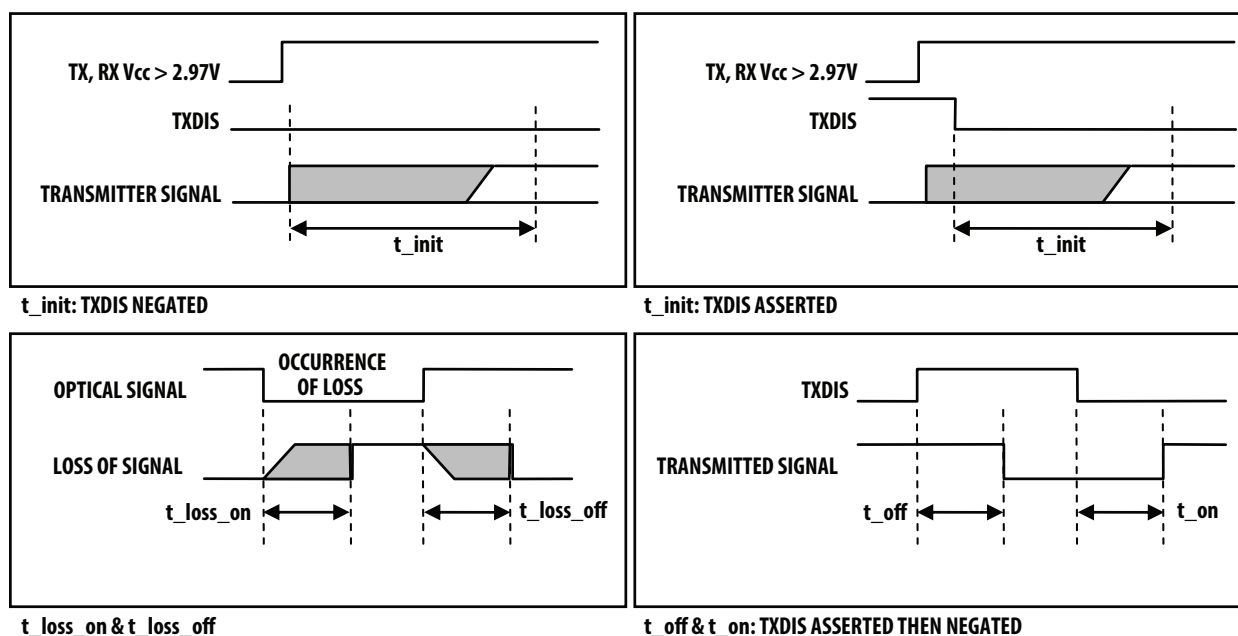


Figure 8. Timing diagrams

Table 10. Transceiver Digital Diagnostic Monitor (Read Time Sense) Characteristics.

| Parameter | Symbol | Max | Units | Notes |
|---|-------------------|------|-------|--|
| Transceiver Internal Temperature Accuracy | T _{INT} | ±3.0 | °C | Registers indicate case temperature which is derived from the internally measured temperature. Valid from -40°C to +85°C case temperature with Tx Enabled. |
| Transceiver Internal Supply Voltage Accuracy | V _{INT} | ±0.1 | V | Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP V _{CC} pin. Valid over 3.3V ±10%. |
| Transmitter LED DC Bias Current Accuracy | I _{BIAS} | ±10 | % | I _{BIAS} is better than ±10% nominal value |
| Transmitter Average Optical Power Accuracy | P _T | ±3.0 | dB | Transmitter power is inferred from the LED bias current. |
| Received Average Optical Input Power Accuracy | P _R | ±3.0 | dB | Coupled from a 62.5/125µm fiber. |

Table 11. EEPROM Serial ID Memory Contents – Address A0h

| Byte # | | | | Byte # | | | |
|---------|-----|-------|-----------------------|----------|-----|-------|--|
| Decimal | Hex | ASCII | Description | Decimal | Hex | ASCII | Description |
| 0 | 03 | | SFP transceiver | 38 | 17 | | |
| 1 | 04 | | | 39 | 6A | | |
| 2 | 07 | | LC connector | 40 | 41 | A | |
| 3 | 00 | | | 41 | 46 | F | |
| 4 | 00 | | | 42 | 42 | B | |
| 5 | 00 | | | 43 | 52 | R | |
| 6 | 20 | | 100Base-FX compliance | 44 | 2D | - | |
| 7 | 00 | | | 45 | 35 | 5 | |
| 8 | 00 | | | 46 | 37 | 7 | |
| 9 | 00 | | | 47 | 45 | E | |
| 10 | 00 | | | 48 | 36 | 6 | |
| 11 | 02 | | 4B/5B Encoding | 49 | 41 | A | |
| 12 | 01 | | 100Mbps/s | 50 | 50 | P | |
| 13 | 00 | | | 51 | 5A | Z | |
| 14 | 00 | | | 52 | 20 | | |
| 15 | 00 | | | 53 | 20 | | |
| 16 | C8 | | | 54 | 20 | | |
| 17 | C8 | | | 55 | 20 | | |
| 18 | 00 | | | 56 | 20 | | |
| 19 | 00 | | | 57 | 20 | | |
| 20 | 41 | A | | 58 | 20 | | |
| 21 | 56 | V | | 59 | 20 | | |
| 22 | 41 | A | | 60 | 05 | | Note 1 |
| 23 | 47 | G | | 61 | 1E | | Note 1 |
| 24 | 4F | O | | 62 | 00 | | |
| 25 | 20 | | | 63 | | | Note 4 |
| 26 | 20 | | | 64 | 00 | | |
| 27 | 20 | | | 65 | 12 | | TX Disable and LOS implemented. |
| 28 | 20 | | | 66 | 00 | | |
| 29 | 20 | | | 67 | 00 | | |
| 30 | 20 | | | 68 - 83 | | | Note 2 |
| 31 | 20 | | | 84 - 91 | | | Note 3 |
| 32 | 20 | | | 92 | 68 | | Digital diagnostics implemented. Internally calibrated. Average RX Power. |
| 33 | 20 | | | 93 | D0 | | Alarm warnings, SoftTX_Disable and Soft RX_LOS implemented. |
| 34 | 20 | | | 94 | 06 | | Includes functionality described in Rev 11.3 of SFF-8472 |
| 35 | 20 | | | 95 | | | Note 4 |
| 36 | 00 | | | 96 - 127 | 00 | | Note 5 |
| 37 | 00 | | | | | | |

Notes:

1. LED wavelength is represented in 16 unsigned bits. The hex representation of 1310 (nm) is 0x051E.
2. Addresses 68-83 specify a unique module serial number.
3. Addresses 84-91 specify the date code.
4. Address 63 is the checksum for bytes 0-62 and address 95 is the checksum for bytes 64-94. They are calculated (per SFF-8472) and stored prior to product shipment.
5. Addresses 96-127 are vendor specific

Table 12. EEPROM Serial ID Memory Contents - Enhanced Features (Address A2h)

| Byte # Decimal | Notes | Byte # Decimal | Notes | Byte # Decimal | Notes |
|-------------------|--------------------------------------|-------------------|---|-------------------|---------------------------------------|
| 0 | Temp H Alarm MSB ^[1] | 26 | Tx Power L Alarm MSB ^[4] | 104 | Real Time Rx Power MSB ^[5] |
| 1 | Temp H Alarm LSB ^[1] | 27 | Tx Power L Alarm LSB ^[4] | 105 | Real Time Rx Power LSB ^[5] |
| 2 | Temp L Alarm MSB ^[1] | 28 | Tx Power H Warning MSB ^[4] | 106 | Reserved |
| 3 | Temp L Alarm LSB ^[1] | 29 | Tx Power H Warning LSB ^[4] | 107 | Reserved |
| 4 | Temp H Warning MSB ^[1] | 30 | Tx Power L Warning MSB ^[4] | 108 | Reserved |
| 5 | Temp H Warning LSB ^[1] | 31 | Tx Power L Warning LSB ^[4] | 109 | Reserved |
| 6 | Temp L Warning MSB ^[1] | 32 | Rx Power H Alarm MSB ^[5] | 110 | Status/Control – See Table 13 |
| 7 | Temp L Warning LSB ^[1] | 33 | Rx Power H Alarm LSB ^[5] | 111 | Reserved |
| 8 | Vcc H Alarm MSB ^[2] | 34 | Rx Power L Alarm MSB ^[5] | 112 | Flag Bits – See Table 14 |
| 9 | Vcc H Alarm LSB ^[2] | 35 | Rx Power L Alarm LSB ^[5] | 113 | Flag Bits – See Table 14 |
| 10 | Vcc L Alarm MSB ^[2] | 36 | Rx Power H Warning MSB ^[5] | 114 | Reserved |
| 11 | Vcc L Alarm LSB ^[2] | 37 | Rx Power H Warning LSB ^[5] | 115 | Reserved |
| 12 | Vcc H Warning MSB ^[2] | 38 | Rx Power L Warning MSB ^[5] | 116 | Flag Bits – See Table 14 |
| 13 | Vcc H Warning LSB ^[2] | 39 | Rx Power L Warning LSB ^[5] | 117 | Flag Bits – See Table 14 |
| 14 | Vcc L Warning MSB ^[2] | 40-55 | Reserved | 118-127 | Reserved |
| 15 | Vcc L Warning LSB ^[2] | 56-94 | External Calibration Constants ^[6] | 128-247 | Customer Writable |
| 16 | Tx Bias H Alarm MSB ^[3] | 95 | Checksum for Bytes 0-94 ^[7] | 248-255 | Vendor Specific |
| 17 | Tx Bias H Alarm LSB ^[3] | 96 | Real Time Temperature MSB ^[1] | | |
| 18 | Tx Bias L Alarm MSB ^[3] | 97 | Real Time Temperature LSB ^[1] | | |
| 19 | Tx Bias L Alarm LSB ^[3] | 98 | Real Time Vcc MSB ^[2] | | |
| 20 | Tx Bias H Warning MSB ^[3] | 99 | Real Time Vcc LSB ^[2] | | |
| 21 | Tx Bias H Warning LSB ^[3] | 100 | Real Time Tx Bias MSB ^[3] | | |
| 22 | Tx Bias L Warning MSB ^[3] | 101 | Real Time Tx Bias LSB ^[3] | | |
| 23 | Tx Bias L Warning LSB ^[3] | 102 | Real Time Tx Power MSB ^[4] | | |
| 24 | Tx Power H Alarm MSB ^[4] | 103 | Real Time Tx Power LSB ^[4] | | |
| 25 | Tx Power H Alarm LSB ^[4] | | | | |

Notes:

1. Temperature (Temp) is decoded as a 16 bit signed two's complement integer in increments of 1/256°C.
2. Supply Voltage (Vcc) is decoded as a 16 bit unsigned integer in increments of 100 μ V.
3. Tx bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 μ A.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μ W.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μ W.
6. Bytes 56-94 are not intended for use with AFBR-57E6APZ, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

Table 13. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110).

| Bit # | Status/Control Name | Description | Notes |
|-------|---------------------|---|-------|
| 7 | TX_DISABLE State | Digital state of Soft TX_DISABLE | |
| 6 | Soft TX_DISABLE | Read/write bit for changing digital state of TX_DISABLE function. | |
| 5 | Reserved | | |
| 4 | Reserved | | |
| 3 | Reserved | | |
| 2 | Reserved | | |
| 1 | RX_LOS State | Digital state of SFP RX_LOS Output Pin (1 = RX_LOS asserted) | |
| 0 | Data Ready (Bar) | Indicates transceiver is powered and real time sense data is ready (0 = ready). | |

Table 14. EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

| Byte | Bit | Flag Bit Name | Description |
|------|-----|-----------------------|--|
| 112 | 7 | Temp High Alarm | Set when transceiver internal temperature exceeds high alarm threshold. |
| | 6 | Temp Low Alarm | Set when transceiver internal temperature exceeds low alarm threshold. |
| | 5 | Vcc High Alarm | Set when transceiver internal supply voltage exceeds high alarm threshold. |
| | 4 | Vcc Low Alarm | Set when transceiver internal supply voltage exceeds low alarm threshold. |
| | 3 | Tx Bias High Alarm | Set when transceiver LED bias exceeds high alarm threshold. |
| | 2 | Tx Bias Low Alarm | Set when transceiver LED bias exceeds low alarm threshold. |
| | 1 | Tx Power High Alarm | Set when transmitted average optical power exceeds high alarm threshold. |
| | 0 | Tx Power Low Alarm | Set when transmitted average optical power exceeds low alarm threshold. |
| 113 | 7 | Rx Power High Alarm | Set when received average optical power exceeds high alarm threshold. |
| | 6 | Rx Power Low Alarm | Set when received average optical power exceeds low alarm threshold. |
| | 0-5 | Reserved | |
| 116 | 7 | Temp High Warning | Set when transceiver case temperature exceeds high warning threshold. |
| | 6 | Temp Low Warning | Set when transceiver case temperature exceeds low warning threshold. |
| | 5 | Vcc High Warning | Set when transceiver internal supply voltage exceeds high warning threshold. |
| | 4 | Vcc Low Warning | Set when transceiver internal supply voltage exceeds low warning threshold. |
| | 3 | Tx Bias High Warning | Set when transceiver LED bias exceeds high warning threshold. |
| | 2 | Tx Bias Low Warning | Set when transceiver LED bias exceeds low warning threshold. |
| | 1 | Tx Power High Warning | Set when transmitted average optical power exceeds high warning threshold. |
| | 0 | Tx Power Low Warning | Set when transmitted average optical power exceeds low warning threshold. |
| 117 | 7 | Rx Power High Warning | Set when received average optical power exceeds high warning threshold. |
| | 6 | Rx Power Low Warning | Set when received average optical power exceeds low warning threshold. |
| | 0-5 | Reserved | |

Table 15. Settings of Alarm and Warning Thresholds

| | Tx Power (dBm) | Rx Power (dBm) | Transceiver Temperature (°C) | Supply Voltage (V) | Tx Bias current (mA) |
|--------------|----------------|----------------|------------------------------|--------------------|----------------------|
| High Alarm | -11 | -11 | 85 | 3.6 | 120 |
| Low Alarm | -23 | -33 | -40 | 3 | 10 |
| High Warning | -12 | -12 | 80 | 3.5 | 110 |
| Low Warning | -22 | -32 | -35 | 3.1 | 15 |

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